

## VERTICAL MOS TRANSISTOR AND MANUFACTURE THEREOF

Patent Number: JP6151867  
Publication date: 1994-05-31  
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Requested Patent: JP6151867  
Application Number: JP19920303981 19921113  
Priority Number(s):  
IPC Classification: H01L29/784  
EC Classification:  
Equivalents: JP2912508B2

### Abstract

**PURPOSE:** To reduce an ON resistance of a vertical MOS transistor having a trench structure and obtain a high breakdown strength and simplify a process.

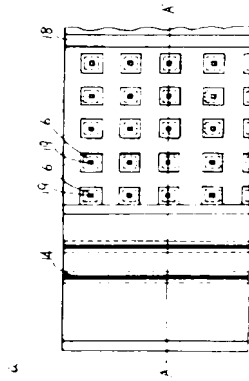
**CONSTITUTION:** P-type well diffusion layers 5 and N-type source diffusion layers 6 formed by stacking the layers in a netted shape and gates of polysilicon layers 4 buried in insulating films 17 of trenches between the layers are installed on the surface of an N-type semiconductor substrate 1. Deep p-type diffusion layers 14 extending below the well diffusion layers 5 of the bottom of the source diffusion layers 6 are installed. The well diffusion layers 5 and the source diffusion layers 6 are formed by an ion implantation and a thermal diffusion.

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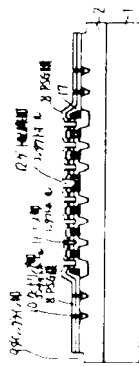




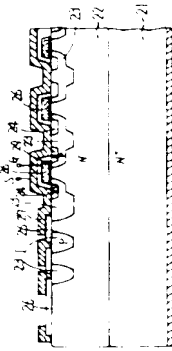
【図1】



【図6】



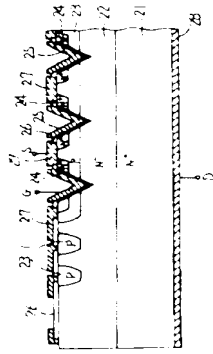
【図9】



【図7】



【図8】



【図10】

